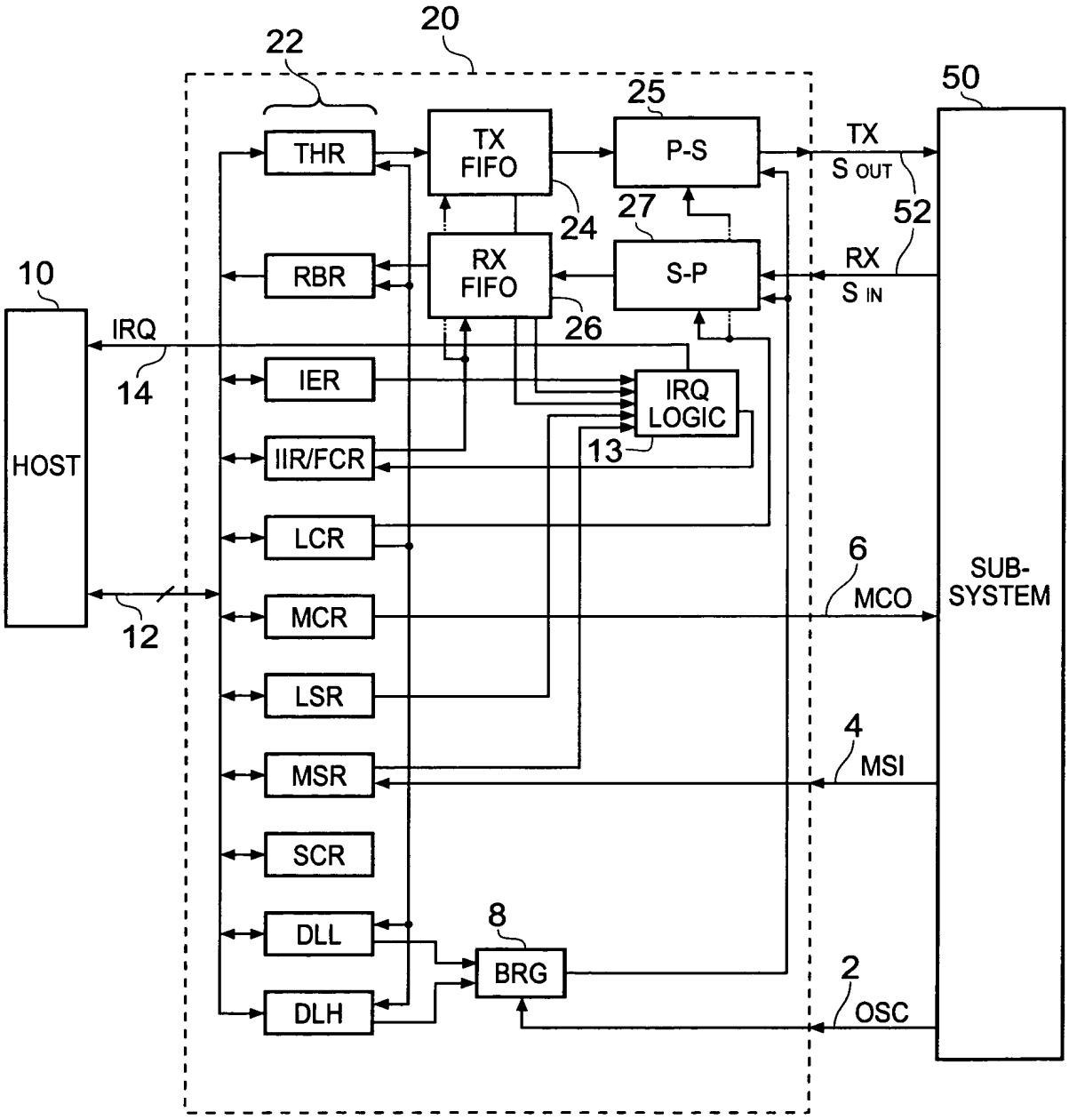
20
22
50
25
THR
TX FIFO
P-S
TX
S OUT
52
24
27
RBR
RX FIFO
S-P
RX
S IN
10
IRQ
14
26
IER
IRQ LOGIC
13
HOST
IIR/FCR
LCR
6
SUB-SYSTEM
MCO
MCR
12
LSR
4
MSI
MSR
SCR
8
DLL
BRG
2
OSC
DLH

Fig. 1

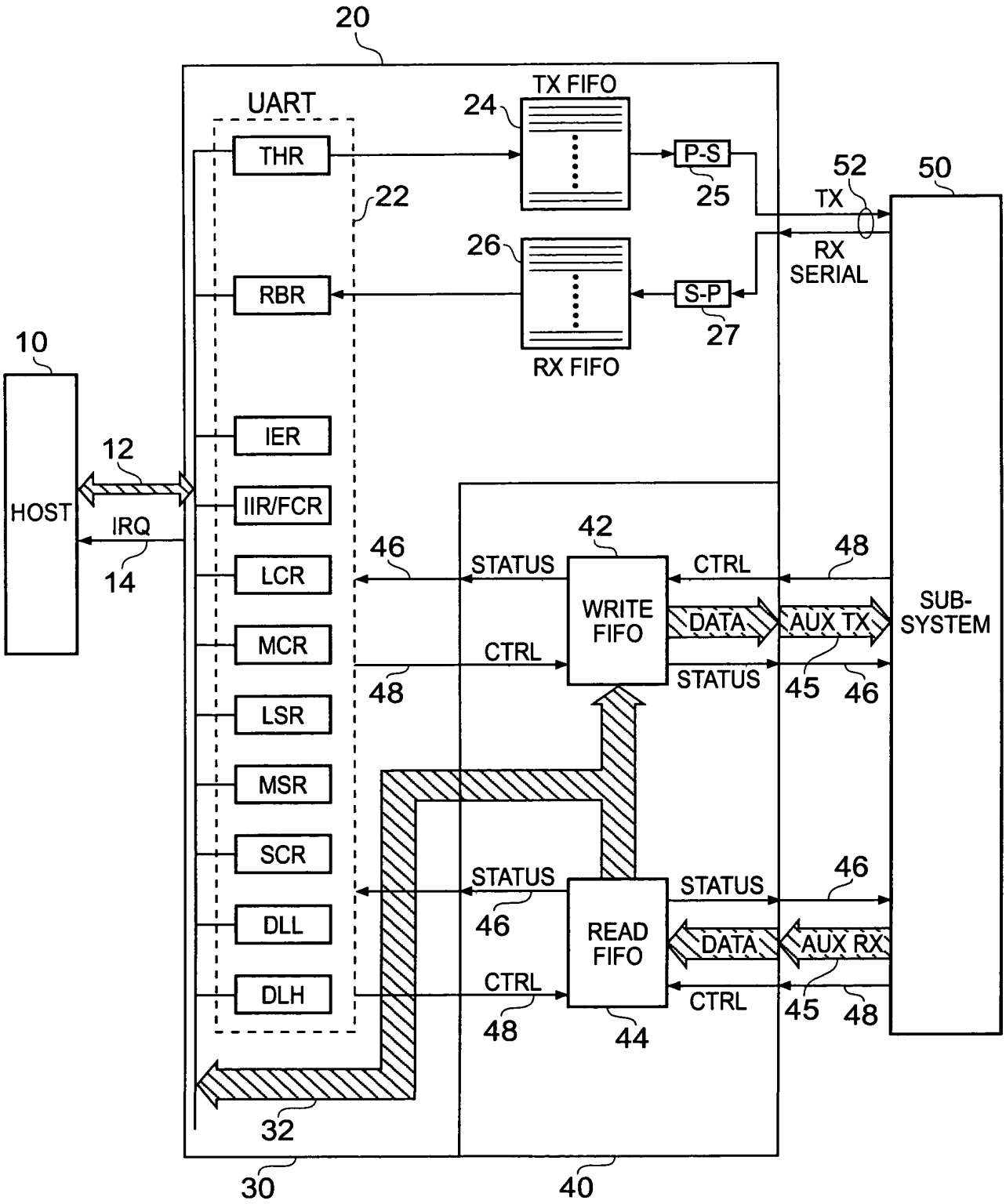
20
UART
THR
RBR
IER
IIR/FCR
LCR
MCR
LSR
MSR
SCR
DLL
DLH
22
TX FIFO
24
P-S
25
26
S-P
27
RX FIFO
52
TX
RX
SERIAL
50
10
HOST
12
IRQ
14
42
WRITE
FIFO
46
STATUS
48
CTRL
DATA
AUX TX
SUB-
SYSTEM
45
46
READ
FIFO
AUX RX
44
32
30
40

Fig. 2

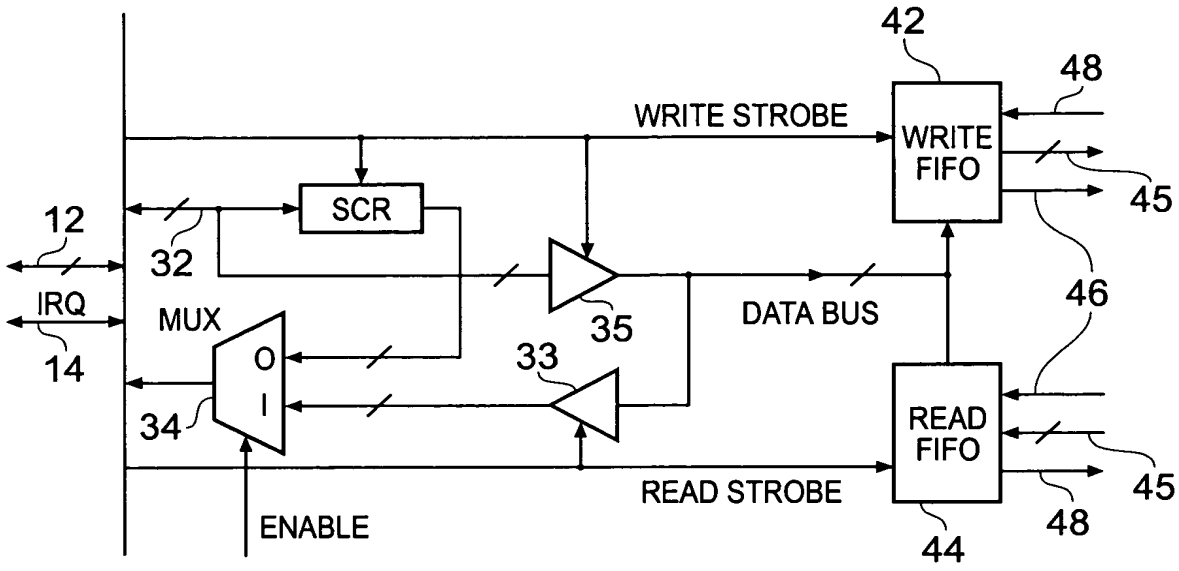

Fig. 3

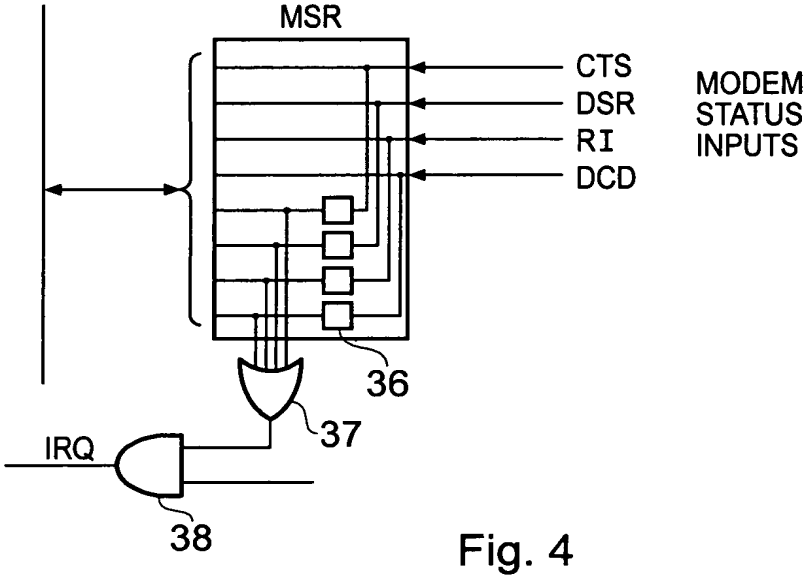

Fig. 4

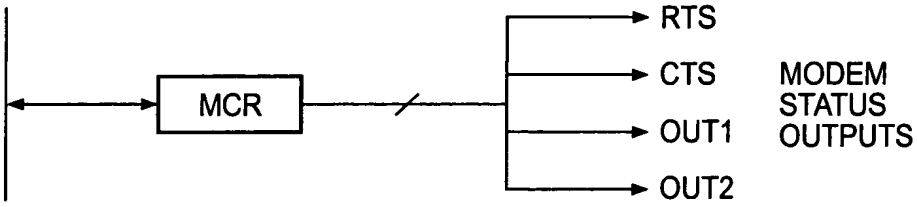

Fig. 5

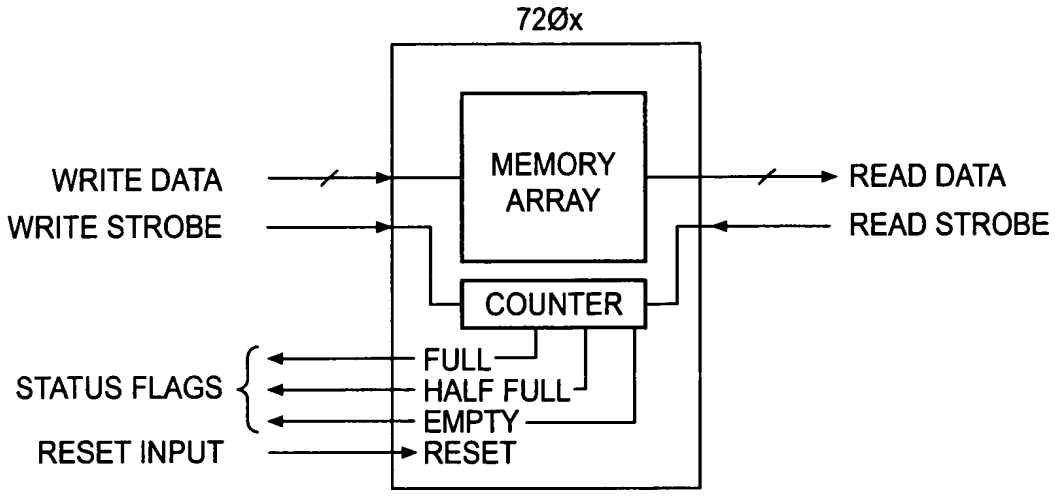
72Øx
MEMORY ARRAY
WRITE DATA
WRITE STROBE
READ DATA
READ STROBE
COUNTER
STATUS FLAGS
FULL
HALF FULL
EMPTY
RESET INPUT
RESET

Fig. 6

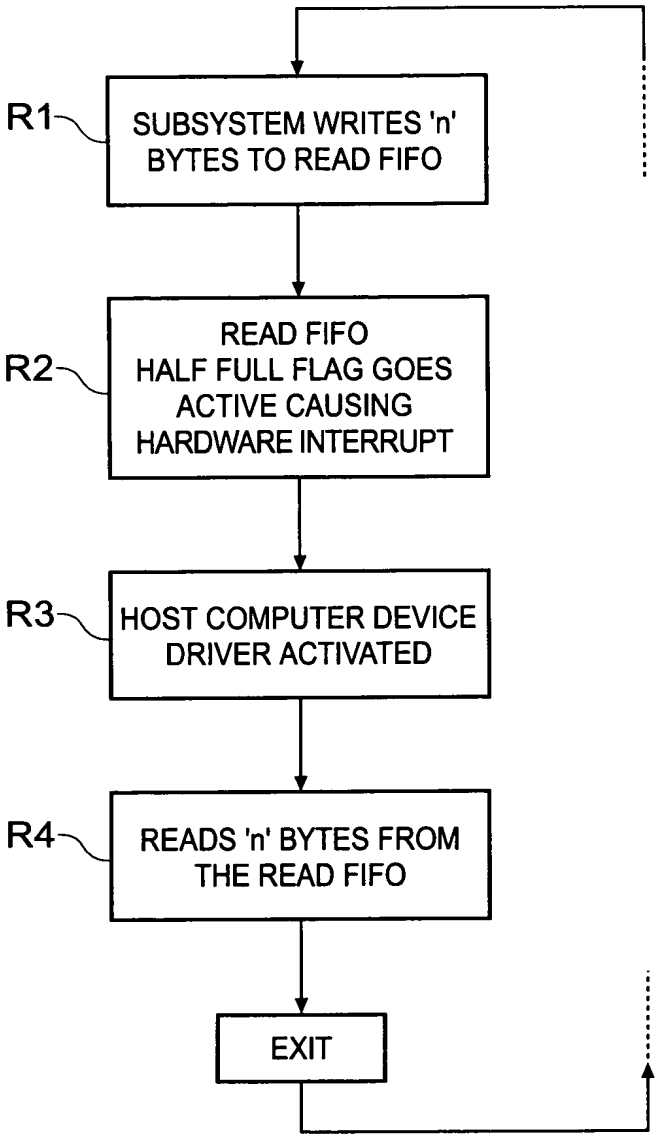
R1
SUBSYSTEM WRITES 'n' BYTES TO READ FIFO
R2
READ FIFO HALF FULL FLAG GOES ACTIVE CAUSING HARDWARE INTERRUPT
R3
HOST COMPUTER DEVICE DRIVER ACTIVATED
R4
READS 'n' BYTES FROM THE READ FIFO
EXIT

Fig. 7

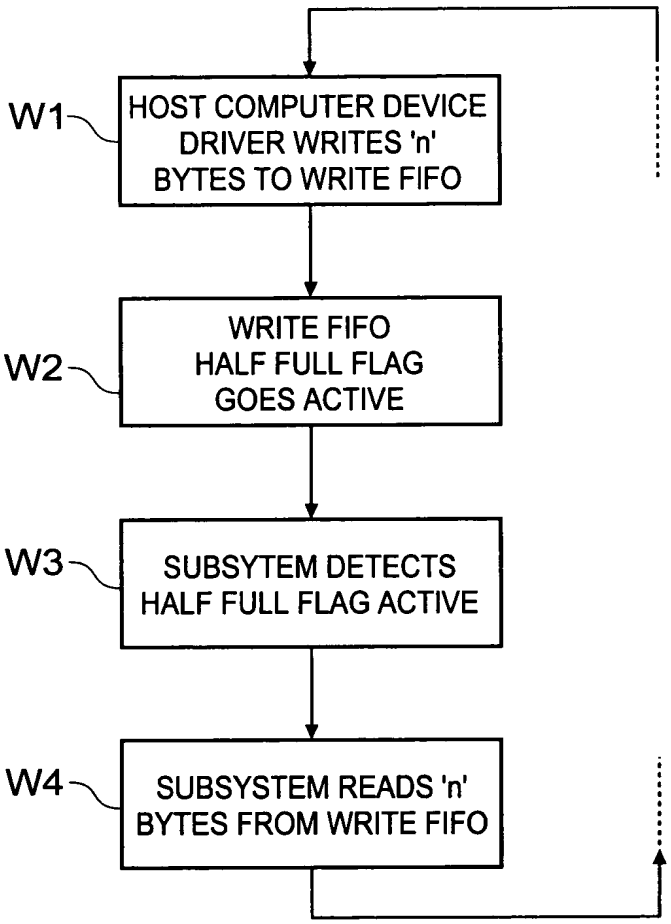
W1
HOST COMPUTER DEVICE DRIVER WRITES 'n' BYTES TO WRITE FIFO
W2
WRITE FIFO HALF FULL FLAG GOES ACTIVE
W3
SUBSYTEM DETECTS HALF FULL FLAG ACTIVE
W4
SUBSYSTEM READS 'n' BYTES FROM WRITE FIFO

Fig. 8

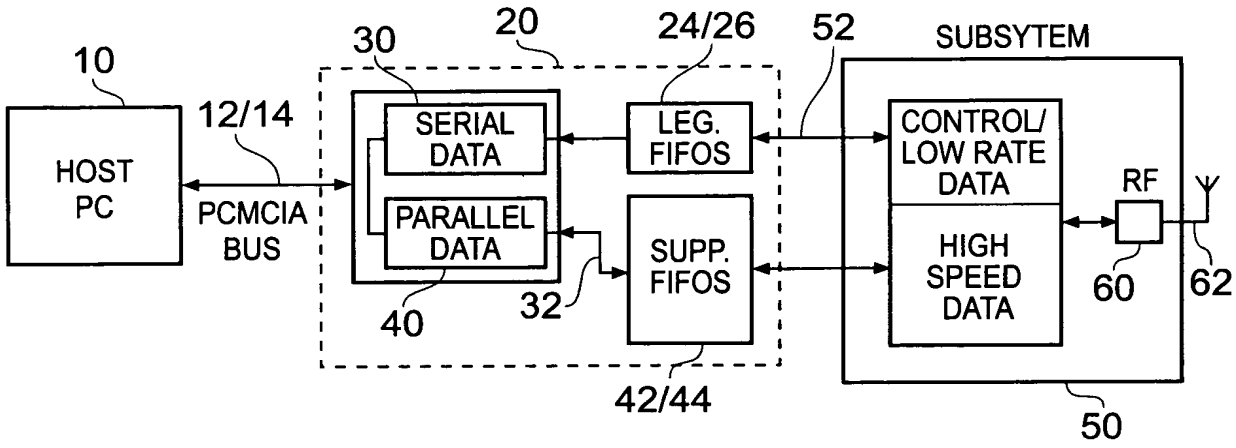
10
HOST PC
12/14
PCMCIA BUS
30
20
24/26
52
SUBSYTEM
SERIAL DATA
PARALLEL DATA
LEG. FIFOS
SUPP. FIFOS
CONTROL/ LOW RATE DATA
HIGH SPEED DATA
RF
60
62
40
32
42/44
50

Fig. 9

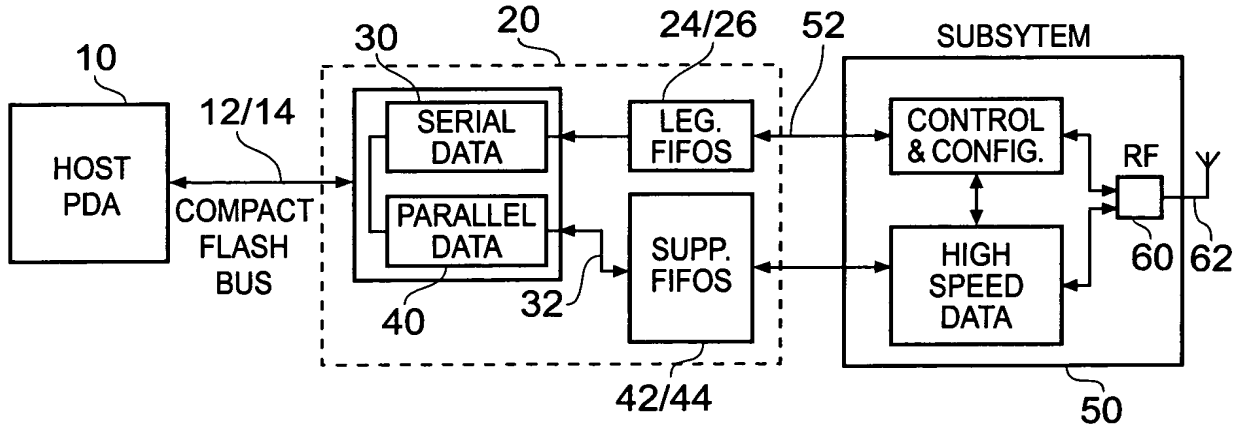
10
HOST PDA
12/14
COMPACT FLASH BUS
30
20
24/26
52
SUBSYTEM
SERIAL DATA
PARALLEL DATA
LEG. FIFOS
SUPP. FIFOS
CONTROL & CONFIG.
HIGH SPEED DATA
RF
60
62
40
32
42/44
50

Fig. 10